Notice of References Cited	Application/Control No. 09/592,207	Applicant(s)/Patent Under Reexamination NAGARASA ET AL.	
	Examiner Albert Wang	Art Unit 2185	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,310,506	10-2001	Brown, David R.	327/284
	B	US-5,670,904	09-1997	Moloney et al.	327/277
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	JP 63177610 A	07-1988	Japan	TSUNEMOTO, TOSHIYUKI	H03K 05/13
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	IBM Technical Disclosure Bulletin, "Programmable Delay Line Control Signal Circuits", Vol. 37, No. 8, pp. 519-520, August 1994.
	V	JEDEC Standard No. 8-6, "High Speed Transceiver Logic (HSTL) - A 1.5 V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits", EIA/JESD8-6, August 1995.
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.